Claims

What is claimed is:

1. A base transistor structure for use in an integrated circuit, the base transistor structure comprising:

a plurality of source regions;

a plurality of drain regions, each adjacent to a corresponding one of the source regions; and

at least first and second elongated gates, the first and second gates each overlying a corresponding subset of the source and drain regions, the first and second gates each extending longitudinally along a first axis from a first end adjacent one of the source and drain regions to a second end extending past another of the source and drain regions, the first and second gates being separated from one another at the second ends thereof;

the base transistor structure being substantially symmetric about the first axis; and

the base transistor structure being configured such that multiple ones of the base transistor structures arranged immediately adjacent to one another are utilizable to form one or more circuit cells of the integrated circuit.

2. The base transistor structure of claim 1 wherein the first and second elongated gates are connectable at the second ends thereof by a conductor formed in a metallization layer of the integrated circuit.

3. The base transistor structure of claim 1 wherein the first and second gates are associated with respective PFET and NFET devices of the base transistor structure.

4. The base transistor structure of claim 1 wherein at least one of the multiple ones of the base transistor structures, arranged immediately adjacent one another, is configurable to provide gate isolation for active transistors in other ones of the base transistor structures.

5. The base transistor structure of claim 1 wherein the first axis corresponds to a y-axis.

6. The base transistor structure of claim 1 wherein the base transistor structure is substantially symmetric about a second axis perpendicular to the first axis.

7. The base transistor structure of claim 1 having a width corresponding approximately to a single grid of a standard cell CAD tool.

8. The base transistor structure of claim 1 wherein the gates are configured so as to permit crossover routing of interconnects within a given one of the circuit cells.

9. The base transistor structure of claim 1 wherein metallization layer connections of the integrated circuit are used to form the circuit cells from the multiple ones of the base transistor structures.

10. The base transistor structure of claim 1 wherein the circuit cells comprise programmable cells of a cell library having a plurality of cells each of which is comprised of multiple ones of the base transistor structure.

11. The base transistor structure of claim 1 wherein a given one of the circuit cells comprises a logic gate formed from a plurality of the base transistor structures.

12. The base transistor structure of claim 1 wherein a given one of the circuit cells comprises a flip-flop circuit formed from a plurality of the base transistor structures.

13. The base transistor structure of claim 1 wherein a plurality of the circuit cells comprise spare gates of the integrated circuit, the spare gates being convertible to active gates using connections formed in a metallization layer of the integrated circuit.

14. The base transistor structure of claim 13 wherein the spare gates are arranged in rows of unused transistors each having the base transistor structure, the rows of unused transistors being interspersed with one or more rows of standard circuit cells.

15. The base transistor structure of claim 1 wherein the circuit cells of the integrated circuit comprise a first plurality of circuit cells each comprising interconnected ones of the base transistor structure and a second plurality of circuit cells each comprising a standard cell not comprising interconnected ones of the base transistor structure.

16. The base transistor structure of claim 15 wherein the second plurality of circuit cells comprise circuit cells of at least a designated type.

17. The base transistor structure of claim 16 wherein the circuit cells of the designated type comprise standard cell flip-flop circuit cells.

18. An integrated circuit comprising:

a plurality of circuit cells, each of at least a subset of the plurality of circuit cells being formed as an interconnection of multiple base transistor structures arranged immediately adjacent to one another;

a given one of the base transistor structures comprising:

a plurality of source regions;

a plurality of drain regions, each adjacent to a corresponding one of the source regions; and

at least first and second elongated gates, the first and second gates each overlying a corresponding subset of the source and drain regions, the first and second gates each extending longitudinally along a first axis from a first end adjacent one of the source and drain regions to a second end extending past another of the source and drain regions, the first and second gates being separated from one another at the second ends thereof;

the base transistor structure being substantially symmetric about the first axis.

19. An article of manufacture comprising one or more software programs for use in designing an integrated circuit, wherein the one or more software programs when executed provide at least a library comprising a plurality of circuit cells, each of at least a subset of the plurality of circuit cells being formed as an interconnection of multiple base transistor structures arranged immediately adjacent to one another, a given one of the base transistor structures comprising:

a given one of the base transistor structures comprising:

a plurality of source regions;

a plurality of drain regions, each adjacent to a corresponding one of the source regions; and

at least first and second elongated gates, the first and second gates each overlying a corresponding subset of the source and drain regions, the first and second gates each extending longitudinally along a first axis from a first end adjacent one of the source and drain regions to a second end extending past another of the source and drain regions, the first and second gates being separated from one another at the second ends thereof;

the base transistor structure being substantially symmetric about the first axis.